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**United States Patent** [19][11] **Patent Number:** **5,774,370****Giomi**[45] **Date of Patent:** **Jun. 30, 1998**

- [54] **METHOD OF EXTRACTING IMPLICIT SEQUENTIAL BEHAVIOR FROM HARDWARE DESCRIPTION LANGUAGES**
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- [51] Int. Cl.<sup>6</sup> ..... G06F 17/50
- [52] U.S. Cl. .... 364/489; 364/488
- [58] Field of Search ..... 364/488, 489, 364/490, 491, 578

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[57] **ABSTRACT**

The method implements implicit sequential behavior using a general finite state machine architecture (FSM) through the systematic evaluation of control flow graphs (CFGs) having one or more weight statements which are sensitive to the same unique clock edge. Each of the weight statements contained in the CFG are assigned a state in the state machine. All of the executable paths between each weight statement are fully evaluated on a node-by-node basis. From this evaluation process, expressions are extracted which define combinational logic necessary to produce additional inputs to the FSM to produce the next state, as well as expressions representing outputs of the FSM as associated with each transition from one state to another. The method also deals with proper evaluation of unrollable loops.

**1 Claim, 31 Drawing Sheets**